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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/602,734	06/25/2003	Amit P. Agrawal	1875.4140000	1520

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EXAMINER	
LEVIN, NAUM B	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 03/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/602,734	AGRAWAL, AMIT P.
	Examiner	Art Unit
	Naum B. Levin	2825

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 June 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 June 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

The drawings filed on 06/25/2003 are acceptable subject to correction of the informalities indicated on the attached "Notice of Draftsperson's Patent Drawing Review," PTO-948. For example, solid shading in Fig.1 does not allow seeing position 113. In order to avoid abandonment of this application, correction is required in reply to the Office action. The correction will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claims 1-10 and 12-19 are rejected under 35 U.S.C. 102(e) as being unpatentable by Cheng et al. (US Patent 6,677,831 B1).

2. As to claims 1 and 13 Cheng discloses:

(1) An apparatus comprising:

an integrated circuit (IC) mounted on a chip carrier (integrated circuit card/printed circuit board/PCB), the IC having one or more differential pair circuits (fiber channel differential signal chip having drivers) coupled thereto, the chip carrier having a signal escaping portion (portion of area 130, where the signal pair exits package pin) and a

remaining portion (portion of area 130, where the signal pair passes through package pin field 130 and expands to a maximum desirable trace width and spacing) (col.1, ll.6-19; col.4, ll.20-23; col.4, ll.41-50; col.5, ll.55-60); and

differential signal lines coupled to the differential pair circuits, the differential signal lines (i) extending through the chip carrier and (ii) having first and second segments (col.2, ll.3-10; col.3, ll.1-6; col.4, ll.39-67);

wherein the first segment extends through the escaping portion and the second segment extends through the remaining portion (col.1, ll.6-19; col.4, ll.20-23; col.4, ll.41-50; col.5, ll.55-60); and

wherein the first and second segments have respective first and second widths (col.2, ll.3-10; col.2, ll.13-24; col.3, ll.1-6; col.4, ll.39-67);

(13) An integrated circuit (IC) (i) having a differential circuit coupled thereto and (ii) mounted on a chip carrier, the differential circuit including a signal escaping portion and a remaining portion, the IC comprising (col.1, ll.6-19; col.4, ll.20-23; col.4, ll.41-50; col.5, ll.55-60):

differential signal lines extending through the chip carrier and including first and second segments (col.2, ll.3-10; col.3, ll.1-6; col.4, ll.39-67);

wherein the first segment extends through the signal escaping portion and the second segment extends through the remaining portion (col.1, ll.6-19; col.4, ll.20-23; col.4, ll.41-50; col.5, ll.55-60);

wherein the first and second segments have respective first and second widths (col.2, ll.3-10; col.2, ll.13-24; col.3, ll.1-6; col.4, ll.39-67); and

wherein the first and second widths provide substantially uniform impedance characteristics across the signal lines (col.2, ll.13-24; col.2, ll.43-50; col.5, ll.62-67; col.6, ll.1-3).

3. As to claims 2-10, 12 and 14-19 Cheng recites:

(2) The apparatus of claim 1, wherein the escaping portion is configured for escaping transmitted signals from the TC (col.2, ll.3-10);

(3), (14) The apparatus/IC, wherein the first and second widths provide substantially uniform impedance characteristics across the signal lines (col.2, ll.43-50; col.5, ll.62-67; col.6, ll.1-3);

(4) The apparatus of claim 3, wherein the impedance is within a range of about 90 to 110 ohm (col.2, ll.60-67; col.4, ll.51-67);

(5), (15) The apparatus/IC, wherein the second width is larger than the first width (col.2, ll.3-10; col.2, ll.13-24; col.3, ll.1-6; col.4, ll.39-67);

(6), (12), (16) The apparatus/IC, wherein the differential signal lines include respective inverting and non-inverting paths, and wherein the paths along the escaping portion are separated by a first spacing and the paths along the remaining portion are separated by at least a second spacing (col.1, ll.20-27; col.2, ll.3-10; col.3, ll.1-6; col.4, ll.39-67);

(7), (17) The apparatus/IC, wherein the second spacing is larger that the first spacing col.2, ll.3-10; col.3, ll.1-6; col.4, ll.39-67);

(8), (18) The apparatus/IC, wherein the first and second spacings cooperate to reduce cross-talk between the inverting and non-inverting paths (col.1, ll.20-27; col.2, ll.3-10; col.3, ll.1-6; col.3, ll.62-67; col.4, ll.39-67);

(9), (19) The apparatus of claim 6, wherein the first and second widths and the first and second spacings are determined based upon modeling and simulations (col.6, ll.38-62);

(10) The apparatus of claim 1, wherein the signal lines are configured to transmit high data rate (speed/frequency) signals (col.1, ll.20-27).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 11 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cheng in view of Lao et al. (US Pub. No.: 20030095014 A1).

As to claims 11 and 20 Cheng teaches the features above but lacks an apparatus for the integrated circuit (IC) design, wherein a data rate of the high data rate signals is greater than or equal to about 5 gigabits per second.

As to claims 11 and 20 Lao discloses:

The apparatus/IC, wherein a data rate of the high data rate signals is greater than or equal to about 5 gigabits per second ([0003]-[0005]; [0053]).

It would have been obvious to a person of ordinary skills in the art at the time the invention was made to employ Lao's teaching regarding the apparatus for the integrated circuit (IC) design, wherein a data rate of the high data rate signals is greater than or equal to about 5 gigabits per second and use it in Cheng's invention in order to properly select an impedance model (e.g. to provide substantially uniform impedance) to achieve desirable rate (speed/frequency) of signals greater or equal to about 5 gigabits per second.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Otsuka et al. (US Patent 6,670,830) discloses a signal transmission bus system that has a transmission line pair on which binary data values are indicated by the presence and absence of a complementary signal. A receiver that senses the presence and absence of the complementary signal on the transmission line pair includes a differential amplifier and a termination transistor coupled across the input terminals of the differential amplifier, to discharge the input capacitance of the differential amplifier so that high-speed signals can be sensed rapidly.

Leddige et al. . (US Pub. No.: 20020079983 A1) recites a printed circuit board. That printed circuit board includes a capacitive load that is coupled to a signal trace. The signal trace has a first section and a second section. The first section is positioned between the capacitive load and the second section. The second section has a first

width, and the first section includes first and second lines that each has a width that is smaller than the first width.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Naum B. Levin whose telephone number is 571-272-1898. The examiner can normally be reached on M-F (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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